

M5M5178BP,J,FP-15,-20

65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This is a family of 8192-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible.

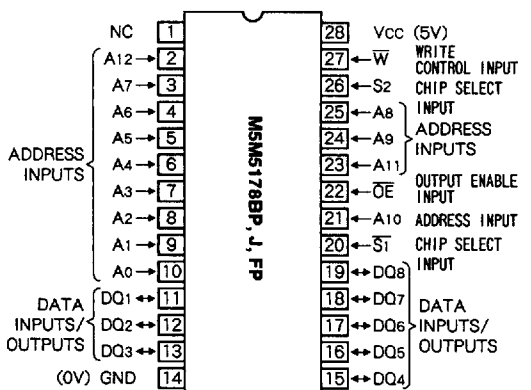
FEATURES

- Fast access time M5M5178BP, J, FP-15..... 15ns(max)
M5M5178BP, J, FP-20..... 20ns(max)
- Single +5V power supply
- Fully static operation: No clocks, no refresh
- Directly TTL compatible: All inputs and outputs
- Three-state outputs: OR-tie capability
- Simple memory expansion by $\overline{S_1}$, S_2
- \overline{OE} prevents data contention in the I/O bus
- Common data I/O

APPLICATION

High-speed memory systems

PIN CONFIGURATION (TOP VIEW)



NC: NO CONNECTION

Outline 28P4Y(P)
28P0J(J)
28P2W-C(FP)

FUNCTION

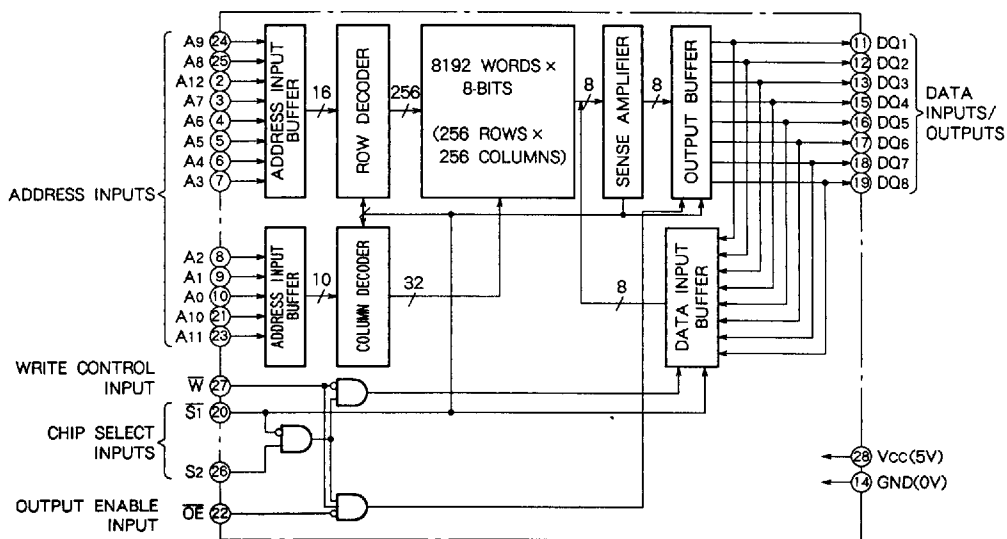
The operation mode of the M5M5178B is determined by a combination of the device control inputs $\overline{S_1}$, S_2 , \overline{W} and \overline{OE} . Each mode is summarized in the function table.(see next page)

A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell

on the trailing edge of \overline{W} , $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1} = L$, $S_2 = H$)

BLOCK DIAGRAM



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When setting $\overline{S_1}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC2} or I_{CC3} .

FUNCTION TABLE

$\overline{S_1}$	S_2	\overline{W}	\overline{OE}	Mode	DQ	I_{CC}
L	L	X	X	Non selection	High-impedance	Active
H	X	X	X	Non selection	High-impedance	Stand by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	- 0.5 * ~7	V
V_I	Input voltage		- 0.5 * ~ V_{CC} + 0.3	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	1000	mW
T_{opr}	Operating temperature		- 10~85	$^\circ\text{C}$
T_{stg}	Storage temperature		- 65~150	$^\circ\text{C}$

DC ELECTRICAL CHARACTERISTICS ($T_a = 0\sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Typ	
V_{IH}	High input voltage		2.4		$V_{CC}+0.3$ V
V_{IL}	Low input voltage		- 0.5*		0.6 V
V_{OH}	High output voltage	$I_{OH} = -4\text{mA}$	2.4		V
V_{OL}	Low output voltage	$I_{OL} = 8\text{mA}$			0.4 V
I_I	Input current	$V_I = 0\sim V_{CC}$			± 10 μA
I_{OZH}	High level output current in off-state	$\overline{S_1} = V_{IH}$ or $S_2 = V_{IL}$ or $\overline{OE} = V_{IH}$			10 μA
I_{OLZ}	Low level output current in off-state	$V_{I/O} = 0\sim V_{CC}$			- 10 μA
I_{CC1}	Active supply current	$\overline{S_1} = V_{IL}$ or $S_2 = V_{IH}$ Output open Other inputs = V_{IH}	AC(25MHz) DC		120 70 mA
I_{CC2}	Stand by supply current	$S_2 = V_{IL}$, $\overline{S_1} = V_{IH}$ Other inputs = $0\sim V_{CC}$	AC(25MHz) DC		30 20 mA
I_{CC3}	Stand by supply current	$\overline{S_1} = V_{CC} - 0.2\text{V}$ Other inputs $\leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V}$			2 mA
C_i	Input capacitance	$\overline{S_1}, S_2, \overline{OE}, \overline{W}$ $A_0\sim A_{12}$	$V_I = \text{GND}$, $V_i = 25\text{mVrms}$, $f = 1\text{MHz}$		7 6 pF
C_o	Output capacitance	$V_O = \text{GND}$, $V_o = 25\text{mVrms}$, $f = 1\text{MHz}$			7 pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)

2. * = -3.0V in case of AC (pulse width $\leq 10\text{ns}$), -0.5V in case of DC

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SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5V \pm 10\%$, unless otherwise noted)**Read cycle**

Symbol	Parameter	Limits						Unit
		M5M5178B-15			M5M5178B-20			
		Min	Typ	Max	Min	Typ	Max	
tCR	Read cycle time	15			20			ns
ta(A)	Address access time			15			20	ns
ta(S1)	Chip select, 1 access time			15			20	ns
ta(S2)	Chip select 2 access time			12			15	ns
ta(OE)	Output enable access time			8			10	ns
tdis(S1)	Output disable time after S1 high			8			10	ns
tdis(S2)	Output disable time after S2 low			8			10	ns
tdis(OE)	Output disable time after OE high			8			10	ns
ten(S1)	Output enable time after S1 low	3			3			ns
ten(S2)	Output enable time after S2 high	2			2			ns
ten(OE)	Output enable time after OE low	2			2			ns
tv(A)	Data valid time after address change	3			3			ns

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{cc} = 5V \pm 10\%$, unless otherwise noted)**Write cycle**

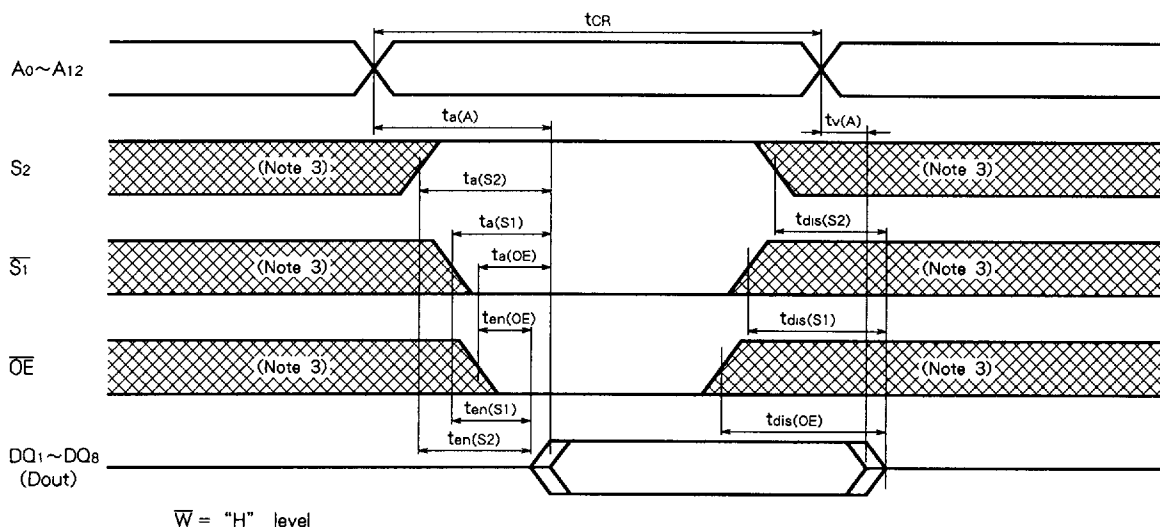
Symbol	Parameter	Limits						Unit
		M5M5178B-15			M5M5178B-20			
		Min	Typ	Max	Min	Typ	Max	
t _{cw}	Write cycle time	15			20			ns
t _{w(W)}	Write pulse width	12			15			ns
t _{su(A)}	Address set up time	0			0			ns
t _{su(S1)}	Chip select 1 set up time	12			16			ns
t _{su(S2)}	Chip select 2 set up time	10			12			ns
t _{su(D)}	Data set up time	8			10			ns
t _{h(D)}	Data hold time	0			0			ns
t _{rec(W)}	Write recovery time	0			0			ns
t _{dis(W)}	Output disable time after \overline{W} low			8			10	ns
t _{dis(OE)}	Output disable time after \overline{OE} high			8			10	ns
t _{en(W)}	Output enable time after \overline{W} high	0			0			ns
t _{en(OE)}	Output enable time after \overline{OE} low	3			3			ns

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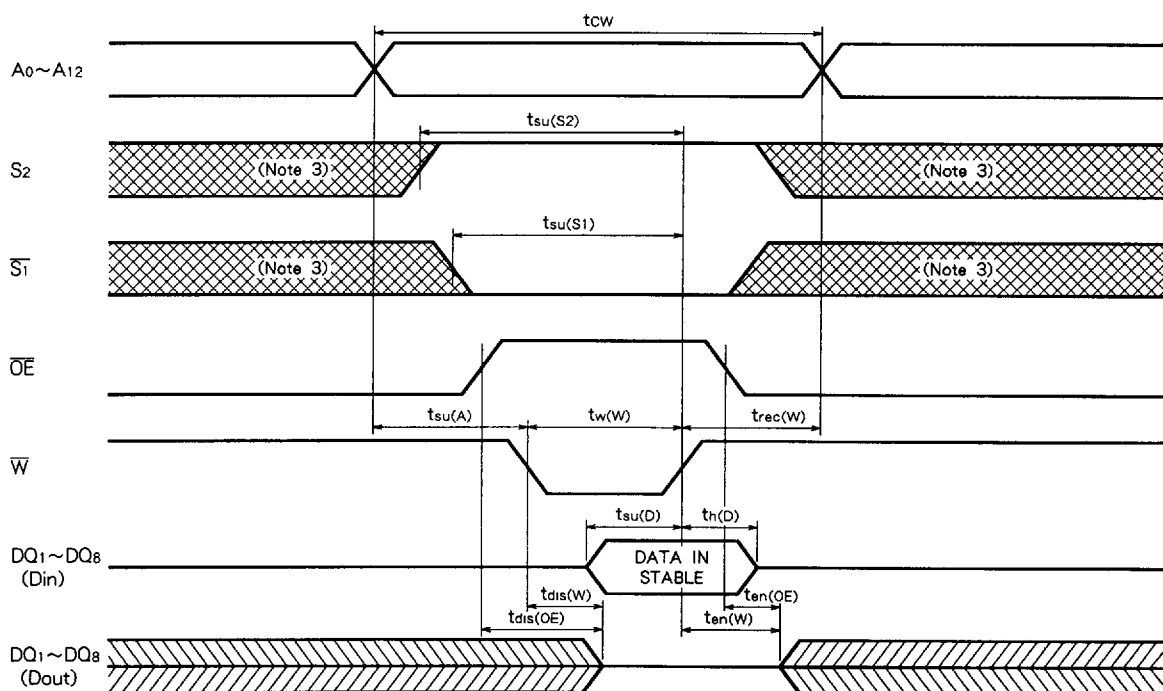
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TIMING DIAGRAM

Read cycle



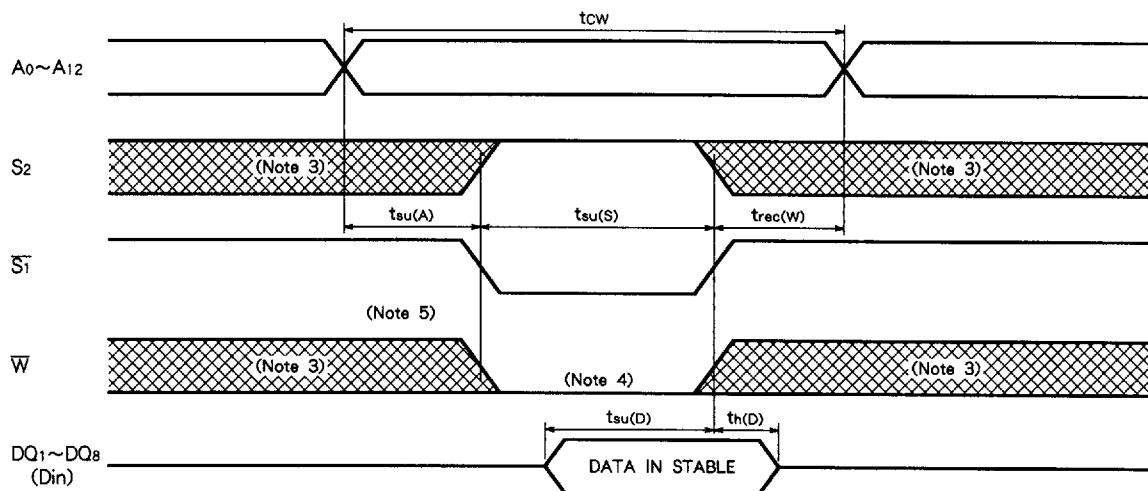
Write cycle (\overline{W} control)



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65536-BIT (8192-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle (\bar{S} control)



CONDITIONS

Input pulse levels..... $V_{IH} = 3V$, $V_{IL} = 0V$
 Input rise and fall time..... 3ns
 Input timing standard levels..... $V_{IH} = V_{IL} = 1.5V$
 Output timing reference levels..... $V_{OH} = V_{OL} = 1.5V$
 Output loads..... Fig. 1, Fig. 2

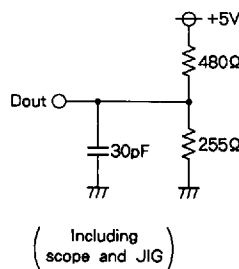
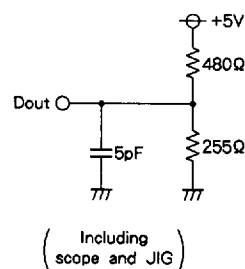


Fig. 1 Output load


Fig. 2 Output load for t_{en} , t_{dis}

Note 3. Hatching indicates the state is don't care.

4. Writing is executed while S_2 high overlaps \bar{S}_T and \bar{W} low.

5. If \bar{W} goes low simultaneously with or prior to \bar{S}_T low or S_2 high, the output remains in the high-impedance state.

6. Don't apply inverted phase signal externally when DQ pin is in output mode.