MICRO POWER SYSTEMS

Operational Amplifiers for Instrumentation

MPOP05 / OP07 / OP10

FEATURES

MPOP05

- Replaces OP-05
- Lowest Noise in the Industry 0.1 Hz to 10 Hz—0.25μVp-p
- Low Bias Current – 0.7nA
- Low V_{OS} – 0.07mV
- High Gain – 500,000
- Fits 725, 108A, 741 Sockets

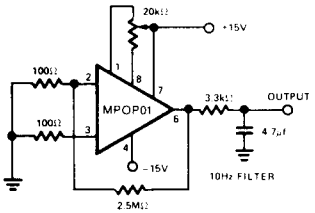
MPOP07

- Replaces OP-07
- Lowest Noise in the Industry 0.1Hz to 10Hz—0.25μVp-p
- Ultra-Low V_{OS} – 10μV
- Ultra-Low V_{OS} Drift – 0.2μV/°C
- Fits 725, 108A, 741, AD510 Sockets

MPOP10

- Replaces OP-10
- Tight V_{OS} Match – 0.07mV
- Tight V_{OS} vs. Temperature Match – 0.45μV/°C
- Tight Bias Current Match – 0.8nA
- Low Noise, 0.1 Hz to 10 Hz – 0.25μVp-p

LOW FREQUENCY NOISE TEST CIRCUIT

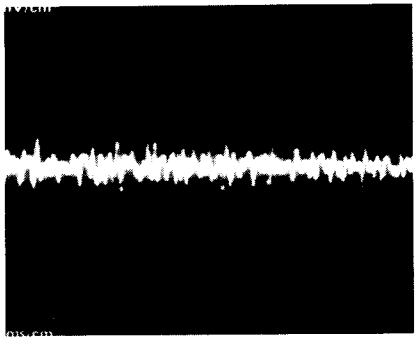


INPUT REF. NOISE $= \frac{V_O}{25{,}000}$

$(en_{p\text{-}p}) = \frac{5mV/cm}{25{,}000}$

$(en_{p\text{-}p}) = 200nV/cm$

TYPICAL MPOP07 NOISE PERFORMANCE



GENERAL DESCRIPTION

Micro Power Systems is pleased to introduce three new series of operational amplifiers. All are designed for convenient application in instrumentation and other low-level signal conditioning circuitry. They are internally compensated and fully protected at input and output, so no additional components are normally needed.

Careful processing and circuit design virtually eliminate low frequency noise, giving these amplifiers a major advantage in limited bandwidth applications. Input bias currents as low as 1na over the full military temperature range are achieved through an internal bias cancellation circuit which supplies most of the bias current needed.

MPOP05

The MPOP05 directly replaces the OP-05, 725, 741, and the 108A. Low initial voltage offset, plus outstanding V_{OS} drift characteristics vs. time and temperature make the MPOP05 ideal for use as buffers, active filters, integrators and sample and hold amplifiers. For applications requiring closely matched performance of dual op-amps, choose the MPOP10.

MPOP07

The MPOP07 is an ultra-low offset voltage op amp with all the performance features mentioned above in the general description. In addition, a V_{OS} of 10μV and TCV_{OS} of 0.2 μV/°C are achieved through permanent alteration of an on-chip offset trimming network during factory test. This extremely low V_{OS} and drift allow the design of equipment requiring minimal recalibration, even after replacement of the op amp. The need for external offset-null components is eliminated. Also, the device's internal frequency compensation and short circuit protection eliminate the need for other external components.

The MPOP07 is an excellent choice for precision amplification of low level transducer signals. Stable integrators, analog computation functions, and precise threshold detectors are easily implemented. It is a superior replacement for many chopper-stabilized amplifiers, and a direct replacement for the OP-07, OP-05, 725, and 108A/308A.

MPOP10

The MPOP10 includes two separate high-performance operational amplifiers, bonded to a common substrate in a 14-pin dual-in-line package. Each individual amplifier meets or exceeds performance of the MPOP05. In addition, the dual MPOP10 features tight matching of all critical parameters, including offset voltage, offset vs. temperature, input bias current, and common mode and power supply rejection ratios.

This dual amplifier is virtually free of the parameter mismatch due to thermal drift encountered in separately packaged amplifiers. Matched parameters allow the design of differential amplifiers with excellent DC characteristics and exceptionally high common mode rejection.

ABSOLUTE MAXIMUM RATINGS

MPOP05, MPOP07, MPOP10 (either side)

Supply Voltage	±22V
Input Voltage[1]	±22V
Differential Input Voltage	±30V
Internal Power Dissipation[2]	500mW
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
MPOP05, A / OP07, A / OP10, A	−55°C to +125°C
MPOP05E, C / OP07E, C, D / OP10E, C	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec.)	300°C

NOTES TO ABSOLUTE MAXIMUM RATINGS

[1] For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

[2] Maximum power dissipation vs. ambient temperature:

Package	Max. Ambient Temp. For Rating	Derate Above Max. Ambient Temp.
TO-99 (J)	80°C	7.1mW/°C
DIP (Y)	100°C	10.0mW/°C
MINI DIP (P)	36°C	5.6mW/°C

ORDERING INFORMATION

MPOP X X X X

BASIC MODEL NUMBER

MPOP05, OP AMP
MPOP07, Low V_{OS} OP AMP
MPOP10, DUAL OP AMP

PACKAGE

J, TO-99
Y, 14-PIN DIP
P, 8-PIN MINI DIP

ELECTRICAL GRADE & TEMP RANGE

0°C TO +70°C

MPOP05E	MPOP07E	MPOP10E
MPOP05C	MPOP07C	MPOP10C
	MPOP07D	

−55°C TO +125°C

MPOP05A	MPOP07A	MPOP10A
MPOP05	MPOP07	MPOP10

DEFINITIONS MP5505 MP5507

Input Offset Voltage (V_{OS})
The voltage required at either input to drive the output to zero volts in a closed loop condition.

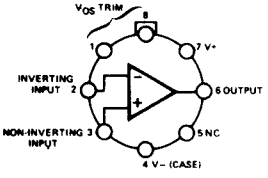
Input Noise Voltage (en_{p-p})
The peak-to-peak noise voltage for a defined bandwidth.

Input Bias Current (I_B)
The average current needed at both input terminals to obtain zero volts at the output.

Common Mode Rejection Ratio (CMRR)
The ratio of the common mode voltage at the inputs, to the resulting voltage error at the output.

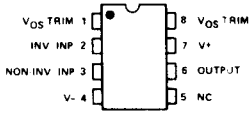
PIN CONNECTIONS (Top View)

MPOP05 and MPOP07



TO-99 (J-SUFFIX)

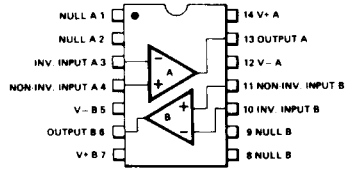
MPOP05 and MPOP07



8-PIN MINI DIP
(P-SUFFIX)

8-PIN CERDIP
(Z SUFFIX)

MPOP10*



14-PIN CERAMIC DIP
(Y-SUFFIX)

*Please note the symmetry of these connections allows the DIP to be plugged in either way: Amplifiers A and B are simply interchanged.

ELECTRICAL CHARACTERISTICS	MPOP05A	MPOP05	

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{OS}		–	0.07	0.15	–	0.2	0.5	mV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 1,2)	–	0.2	1.0	–	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		–	0.7	2.0	–	1.0	2.8	nA
Input Bias Current	I_B		–	±0.7	±2.0	–	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.25	0.5	–	0.25	0.5	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	–	10.3	18.0	–	10.3	18.0	nV/√Hz
		f_o = 100Hz (Note 2)	–	10.0	13.0	–	10.0	13.0	
		f_o = 1000Hz (Note 2)	–	9.6	11.0	–	9.6	11.0	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	14	30	pA p-p
Input Noise Current Density	I_n	f_o = 10Hz (Note 2)	–	0.32	0.80	–	0.32	0.80	pA/√Hz
		f_o = 100Hz (Note 2)	–	0.14	0.23	–	0.14	0.23	
		f_o = 1000Hz (Note 2)	–	0.12	0.17	–	0.12	0.17	
Input Resistance – Diff. Mode	R_{in}		30	80	–	20	60	–	MΩ
Input Resistance – Com. Mode	R_{inCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	114	126	–	114	126	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	110	–	100	110	–	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	300	500	–	200	500	–	V/mV
		R_L ≥ 500Ω, V_O = ±.5V	150	500	–	150	500	–	
		V_S = ±3V							
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10kΩ	±12.5	±13.0	–	±12.5	±13.0	–	V
		R_L ≥ 2kΩ	±12.0	±12.8	–	±12.0	±12.8	–	
		R_L ≥ 1kΩ	±10.5	±12.0	–	±10.5	±12.0	–	
Slewing Rate	SR	R_L ≥ 2kΩ	–	0.17	–	–	0.17	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	60	–	–	60	–	Ω
Power Consumption	P_d		–	90	120	–	90	120	mW
		V_S = ±3V	–	4	6	–	4	6	
Offset Adjustment Range		R_p = 20kΩ	–	±4	–	–	±4	–	mV

The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.10	0.24	–	0.3	0.7	mV
Average V_{OS} Drift									μV/°C
Without External Trim	TCV_{OS}		–	0.3	0.9	–	0.7	2.0	
With External Trim	TCV_{OSn}	R_p = 20kΩ	–	0.2	0.5	–	0.3	1.0	
Input Offset Current	I_{OS}		–	1.0	4.0	–	1.8	5.6	nA
Average I_{OS} Drift	TCI_{OS}		–	5	25	–	8	50	pA/°C
Input Bias Current	I_B		–	±1.0	±4.0	–	±2.0	±6.0	nA
Average I_B Drift	TCI_B		–	8	25	–	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	123	–	110	123	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	106	–	94	106	–	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	200	400	–	150	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 2kΩ	±12.0	±12.6	–	±12.0	±12.6	–	V

ELECTRICAL CHARACTERISTICS	MPOP05E	MPOP05C	

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{OS}		–	0.2	0.5	–	0.3	1.3	mV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 1,2)	–	0.3	1.5	–	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		–	1.2	3.8	–	1.8	6.0	nA
Input Bias Current	I_B		–	±1.2	±4.0	–	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.25	0.5	–	0.25	0.5	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	–	10.3	18.0	–	10.5	20.0	nV/√Hz
		f_o = 100Hz (Note 2)	–	10.0	13.0	–	10.2	13.5	
		f_o = 1000Hz (Note 2)	–	9.6	11.0	–	9.8	11.5	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	15	35	pA p-p
Input Noise Current Density	I_n	f_o = 10Hz (Note 2)	–	0.32	0.80	–	0.35	0.90	pA/√Hz
		f_o = 100Hz (Note 2)	–	0.14	0.23	–	0.15	0.27	
		f_o = 1000Hz (Note 2)	–	0.12	0.17	–	0.13	0.18	
Input Resistance – Diff. Mode	R_{in}		15	50	–	8	33	–	MΩ
Input Resistance – Com. Mode	R_{inCM}		–	160	–	–	120	–	GΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	123	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	107	–	90	104	–	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	200	500	–	120	400	–	V/mV
		R_L ≥ 500Ω, V_O = ±.5V	150	500	–	100	400	–	
		V_S = ±3V							
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 10kΩ	±12.5	±13.0	–	±12.0	±13.0	–	V
		R_L ≥ 2kΩ	±12.0	±12.8	–	±11.5	±12.8	–	
		R_L ≥ 1kΩ	±10.5	±12.0	–	–	±12.0	–	
Slewing Rate	SR	R_L ≥ 2kΩ	–	0.17	–	–	0.17	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	60	–	–	60	–	Ω
Power Consumption	P_d		–	90	120	–	95	150	mW
		V_S = ±3V	–	4	6	–	4	8	
Offset Adjustment Range		R_p = 20kΩ	–	±4	–	–	±4	–	mV

The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.25	0.6	–	0.35	1.6	mV
Average V_{OS} Drift									μV/°C
Without External Trim	TCV_{OS}	(Note 2)	–	0.7	2.0	–	1.2	4.5	
With External Trim	TCV_{OSn}	R_p = 20kΩ (Note 2)	–	0.2	0.6	–	0.4	1.5	
Input Offset Current	I_{OS}		–	1.4	5.3	–	2.0	8.0	nA
Average I_{OS} Drift	TCI_{OS}	(Note 2)	–	8	35	–	12	50	pA/°C
Input Bias Current	I_B		–	±1.5	±5.5	–	±2.2	±9.0	nA
Average I_B Drift	TCI_B	(Note 2)	–	13	35	–	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	107	123	–	97	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	90	104	–	86	100	–	dB
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	180	450	–	100	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	R_L ≥ 2kΩ	±12.0	±12.6	–	±11.0	±12.6	–	V

ELECTRICAL CHARACTERISTICS			MPOP07A			MPOP07			

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{OS}		–	10	25	–	30	75	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 1,2)	–	0.2	1.0	–	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		–	0.3	2.0	–	0.4	2.8	nA
Input Bias Current	I_B		–	±0.7	±2.0	–	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.25	0.5	–	0.25	0.5	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	–	10.3	18.0	–	10.3	18.0	nV/√Hz
		f_o = 100Hz (Note 2)	–	10.0	13.0	–	10.0	13.0	
		f_o = 1000Hz (Note 2)	–	9.6	11.0	–	9.6	11.0	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	14	30	pA p-p
Input Noise Current Density	I_n	f_o = 10Hz (Note 2)	–	0.32	0.80	–	0.32	0.80	pA/√Hz
		f_o = 100Hz (Note 2)	–	0.14	0.23	–	0.14	0.23	
		f_o = 1000Hz (Note 2)	–	0.12	0.17	–	0.12	0.17	
Input Resistance – Diff. Mode	R_{in}		30	80	–	20	60	–	MΩ
Input Resistance – Com. Mode	R_{inCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	110	126	–	110	126	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	100	110	–	100	110	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	–	200	500	–	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm .5V$, $V_S = \pm 3V$	150	500	–	150	500	–	
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	±12.5	±13.0	–	±12.5	±13.0	–	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	–	±12.0	±12.8	–	
		$R_L \geq 1k\Omega$	±10.5	±12.0	–	±10.5	±12.0	–	
Slewing Rate	SR	$R_L \geq 2k\Omega$	–	0.17	–	–	0.17	–	V/μsec
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	–	60	–	–	60	–	Ω
Power Consumption	P_d		–	75	120	–	75	120	mW
		$V_S = \pm 3V$	–	4	6	–	4	6	
Offset Adjustment Range		$R_p = 20k\Omega$	–	±4	–	–	±4	–	mV

The following specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	25	60	–	60	200	μV
Average V_{OS} Drift									μV/°C
Without External Trim	TCV_{OS}		–	0.2	0.6	–	0.3	1.3	
With External Trim	TCV_{OSn}	$R_p = 20k\Omega$	–	0.2	0.6	–	0.3	1.3	
Input Offset Current	I_{OS}		–	0.8	4.0	–	1.2	5.6	nA
Average I_{OS} Drift	TCI_{OS}		–	5	25	–	8	50	pA/°C
Input Bias Current	I_B		–	±1.0	±4.0	–	±2.0	±6.0	nA
Average I_B Drift	TCI_B		–	8	25	–	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	106	123	–	106	123	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	94	106	–	94	106	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	–	150	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±12.0	±12.6	–	±12.0	±12.6	–	V

NOTE 1: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
NOTE 2: This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.

ELECTRICAL CHARACTERISTICS	MPOP07E	MPOP07C	MPOP07D	

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{OS}		–	30	75	–	60	150	–	60	150	μV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 1,2)	–	0.3	1.5	–	0.4	2.0	–	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		–	0.5	3.8	–	0.8	6.0	–	0.8	6.0	nA
Input Bias Current	I_B		–	±1.2	±4.0	–	±1.8	±7.0	–	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.25	0.5	–	0.25	0.5	–	0.25	0.5	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2) f_o = 100Hz (Note 2) f_o = 1000Hz (Note 2)	– – –	10.3 10.0 9.6	18.0 13.0 11.0	– – –	10.5 10.2 9.8	20.0 13.5 11.5	– – –	10.5 10.2 9.8	20.0 13.5 11.5	nV/√Hz
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	15	35	–	15	35	pAp-p
Input Noise Current Density	I_n	f_o = 10Hz (Note 2) f_o = 100Hz (Note 2) f_o = 1000Hz (Note 2)	– – –	0.32 0.14 0.12	0.80 0.23 0.17	– – –	0.35 0.15 0.13	0.90 0.27 0.18	– – –	0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
Input Resistance – Diff. Mode	R_{in}		15	50	–	8	33	–	7	31	–	MΩ
Input Resistance – Com. Mode	R_{inCM}		–	160	–	–	120	–	–	120	–	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	–	±13.0	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	–	100	120	–	94	110	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	107	–	90	104	–	90	104	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq$ 2kΩ, V_O = ±10V $R_L \geq$ 500Ω, V_O = ±.5V V_S = ±3V	200 150	500 500	– –	120 100	400 400	– –	120 –	400 –	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq$ 10kΩ $R_L \geq$ 2kΩ $R_L \geq$ 1kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	– – –	±12.0 ±11.5 –	±13.0 ±12.8 ±12.0	– – –	±12.0 ±11.5 –	±13.0 ±12.8 –	– – –	V
Slewing Rate	SR	$R_L \geq$ 2kΩ	–	0.17	–	–	0.17	–	–	0.17	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.6	–	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	60	–	–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±3V	– –	75 4	120 6	– –	80 4	150 8	– –	80 4	150 8	mW
Offset Adjustment Range		R_p = 20kΩ	–	±4	–	–	±4	–	–	±4	–	mV

The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	45	130	–	85	250	–	85	250	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 (Note 2) R_p = 20kΩ (Note 2)	 – –	 0.3 0.3	 1.3 1.3	 – –	 0.5 0.4	 1.8 1.6	 – –	 0.7 0.7	 2.5 2.5	μV/°C
Input Offset Current	I_{OS}		–	0.9	5.3	–	1.6	8.0	–	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	8	35	–	12	50	–	12	50	pA/°C
Input Bias Current	I_B		–	±1.5	±5.5	–	±2.2	±9.0	–	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	13	35	–	18	50	–	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	103	123	–	97	120	–	94	106	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	90	104	–	86	100	–	86	100	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq$ 2kΩ, V_O = ±10V	180	450	–	100	400	–	100	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq$ 2kΩ	±12.0	±12.6	–	±11.0	±12.6	–	±11.0	±12.6	–	V

MATCHING CHARACTERISTICS	MPOP10A	MPOP10	

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Input Offset Voltage Match	ΔV_{OS}		–	0.07	0.18	–	0.12	0.5	mV
Average Non-Inverting Bias Current	I_{B+}		–	±1.0	±3.0	–	±1.3	±4.5	nA
Non-Inverting Offset Current	I_{OS+}		–	0.8	2.8	–	1.1	4.5	nA
Inverting Offset Current	I_{OS-}		–	0.8	2.8	–	1.1	4.5	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±CMVR	114	123	–	106	120	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	V_S = ±3V to ±18V	100	112	–	94	110	–	dB
Channel Separation			126	140	–	126	140	–	dB

These specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

Input Offset Voltage Match	ΔV_{OS}		–	0.10	0.30	–	0.20	0.90	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 2)	–	0.45	1.3	–	0.9	2.5	μV/°C
With External Trim	$TC\Delta V_{OSn}$	R_p = 20kΩ (Note 2) Channel A only See Applications	–	0.3	0.8	–	0.4	1.2	μV/°C
Average Non-Inverting Bias Current	I_{B+}		–	±2.0	±6.0	–	±2.4	±8.0	nA
Average Drift of Non-Inverting Bias Current	TCI_{B+}		–	10	40	–	15	–	pA/°C
Non-Inverting Offset Current	I_{OS+}		–	2.0	6.5	–	2.4	9.0	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS+}		–	12	50	–	18	–	pA/°C
Inverting Offset Current	I_{OS-}		–	2.0	6.5	–	2.4	9.0	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±CMVR	108	120	–	103	117	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	V_S = ±3V to ±18V	94	105	–	90	103	–	dB

Note 1: Exclude first hour of operation to allow for stabilization of external circuitry.
Note 2: This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.

INDIVIDUAL AMPLIFIER CHARACTERISTICS	MPOP10A	MPOP10	

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{OS}		–	0.2	0.5	–	0.2	0.5	mV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 1,2)	–	2.5	9	–	2.5	9	μV/Mo
Input Offset Current	I_{OS}		–	1.0	2.8	–	1.0	2.8	nA
Input Bias Current	I_B		–	±1.0	±3.0	–	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.25	0.5	–	0.25	0.5	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	–	10.3	18.0	–	10.3	18.0	nV/√Hz
		f_o = 100Hz (Note 2)	–	10.0	13.0	–	10.0	13.0	
		f_o = 1000Hz (Note 2)	–	9.6	11.0	–	9.6	11.0	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	14	30	pA p-p

INDIVIDUAL AMPLIFIER CHARACTERISTICS, Continued

			MPOP10A			MPOP10			
Input Noise Current Density	I_n	f_o = 10Hz (Note 2) f_o = 100Hz (Note 2) f_o = 1000Hz (Note 2)	– – –	0.32 0.14 0.12	0.80 0.23 0.17	– – –	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance – Diff. Mode	R_{in}		20	60	–	20	60	–	MΩ
Input Resistance – Com. Mode	R_{inCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	126	–	110	126	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	110	–	100	110	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ±.5V V_S = ±3V	200 150	500 500	– –	200 150	500 500	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	– – –	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	– – –	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	–	0.17	–	–	0.17	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1 0	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	60	–	–	60	–	Ω
Power Consumption	P_d	 V_S = ±3V	– –	90 4	120 6	– –	90 4	120 6	mW
Offset Adjustment Range		R_p = 20kΩ	–	±4	–	–	±4	–	mV
Input Capacitance	C_{in}		–	8	–	–	8	–	pF

The following specifications apply for V_S = ±15V, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.3	0.7	–	0.3	0.7	mV
Average V_{OS} Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 R_p = 20kΩ (Note 2) R_p = 20kΩ (Note 2)	 – –	 0.7 0.3	 2.0 1.0	 – –	 0.7 0.3	 2.0 1.0	μV/°C
Input Offset Current	I_{OS}		–	1.8	5.6	–	1.8	5.6	nA
Average I_{OS} Drift	TCI_{OS}		–	8	50	–	8	50	pA/°C
Input Bias Current	I_B		–	±2.0	±6.0	–	±2.0	±6.0	nA
Average I_B Drift	TCI_B		–	13	50	–	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	–	106	123	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	106	–	94	106	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	150	400	–	150	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±12.0	±12.6	–	±12.0	±12.6	–	V

NOTE 1: Exclude first hour of operation to allow for stabilization of external circuitry.
NOTE 2: This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.

MATCHING CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	MPOP10E Min.	MPOP10E Typ.	MPOP10E Max.	MPOP10C Min.	MPOP10C Typ.	MPOP10C Max.	Units
Input Offset Voltage Match	ΔV_{OS}		–	0.12	0.5	–	0.3	–	mV
Average Non-Inverting Bias Current	I_{B+}		–	±1.3	±4.5	–	±2.0	–	nA

MATCHING CHARACTERISTICS, Continued

			MPOP10E			MPOP10C			
Non-Inverting Offset Current	I_{OS+}		–	1.1	4.5	–	1.8	–	nA
Inverting Offset Current	I_{OS-}		–	1.1	4.5	–	1.8	–	nA
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±CMVR	106	120	–	–	117	–	dB
Power Supply Rejection Ratio Match	ΔPSRR	V_S = ±3V to ±18V	94	110	–	–	106	–	dB
Channel Separation			126	140	–	120	137	–	dB

These specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

Input Offset Voltage Match	ΔV_{OS}		–	0.18	0.7	–	0.4	–	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$		–	0.9	2.3 (Note 1)	–	1.3	–	μV/°C
With External Trim	$TC\Delta V_{OSn}$	R_p = 20kΩ Channel A only See Applications	–	0.3	0.9	–	0.6	–	μV/°C
Average Non-Inverting Bias Current	I_{B+}		–	±2.0	±6.0	–	±2.8	–	nA
Average Drift of Non-Inverting Bias Current	TCI_{B+}		–	12	40 (Note 2)	–	18	–	pA/°C
Non-Inverting Offset Current	I_{OS+}		–	2.0	6.0	–	2.8	–	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS+}		–	15	50 (Note 2)	–	20	–	pA/°C
Inverting Offset Current	I_{OS-}		–	2.0	6.0	–	2.8	–	nA
Common Mode Rejection Ratio Match	ΔCMRR		103	117	–	–	114	–	dB
Power Supply Rejection Ratio Match	ΔPSRR		90	105	–	–	102	–	dB

Note 1: Exclude first hour of operation to allow for stabilization of external circuitry.
Note 2: This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.

INDIVIDUAL AMPLIFIER CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	MPOP10E Min.	MPOP10E Typ.	MPOP10E Max.	MPOP10C Min.	MPOP10C Typ.	MPOP10C Max.	Units
Input Offset Voltage	V_{OS}		–	0.2	0.5	–	0.3	1.3	mV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 1,2)	–	2.5	9	–	3.5	–	μV/Mo
Input Offset Current	I_{OS}		–	1.2	3.8	–	1.8	6.0	nA
Input Bias Current	I_B		–	±1.2	±4.0	–	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.25	0.5	–	0.25	0.5	μVp-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	–	10.3	18.0	–	10.5	20.0	nV/√Hz
		f_o = 100Hz (Note 2)	–	10.0	13.0	–	10.2	13.5	
		f_o = 1000Hz (Note 2)	–	9.6	11.0	–	9.8	11.5	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	15	35	pA p-p
Input Noise Current Density	I_n	f_o = 10Hz (Note 2)	–	0.32	0.80	–	0.35	0.90	pA/√Hz
		f_o = 100Hz (Note 2)	–	0.14	0.23	–	0.15	0.27	
		f_o = 1000Hz (Note 2)	–	0.12	0.17	–	0.13	0.18	
Input Resistance – Diff. Mode	R_{in}		15	50	–	8	33	–	MΩ
Input Resistance – Com. Mode	R_{inCM}		–	160	–	–	120	–	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	–	100	120	–	dB

INDIVIDUAL AMPLIFIER CHARACTERISTICS, Continued

			MPOP10E			MPOP10C			
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	94	107	–	90	104	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 5V$ $V_S = \pm 3V$	200 150	500 500	– –	120 100	400 400	– –	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	– – –	±12.0 ±11.5 –	±13.0 ±12.8 ±12.0	– – –	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	–	0.17	–	–	0.17	–	V/μsec
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	–	60	–	–	60	–	Ω
Power Consumption	P_d	 $V_S = \pm 3V$	– –	90 4	120 6	– –	95 4	150 8	mW
Offset Adjustment Range		$R_p = 20k\Omega$	–	±4	–	–	±4	–	mV
Input Capacitance	C_{in}		–	–	–	–	8	–	pF

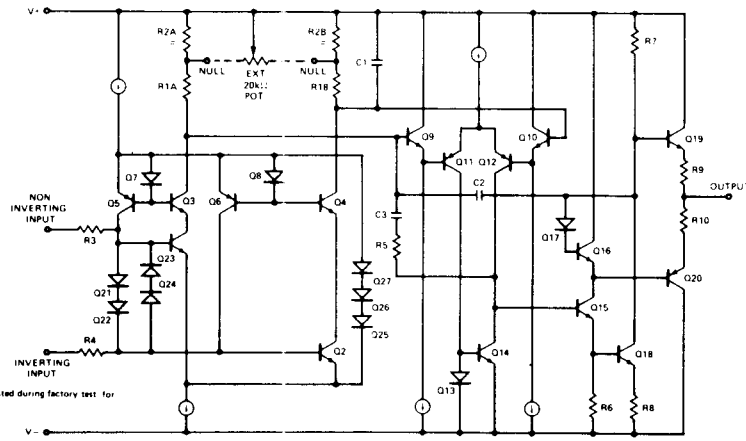
The following specifications apply for $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

Input Offset Voltage	V_{OS}		–	0.25	0.6	–	0.35	1.6	mV
Average V_{OS} Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 (Note 2) $R_p = 20k\Omega$ (Note 2)	 – –	 0.7 0.3	 2.0 1.0	 – –	 1.2 0.4	 4.5 1.5	μV/°C
Input Offset Current	I_{OS}		–	1.4	5.3	–	2.0	8.0	nA
Average I_{OS} Drift	TCI_{OS}	(Note 2)	–	8	35	–	12	50	pA/°C
Input Bias Current	I_B		–	±1.5	±5.5	–	+2.2	+9.0	nA
Average I_B Drift	TCI_B	(Note 2)	–	13	35	–	18	50	pA/°C
Input Voltage Range	CMVR		+13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	103	123	–	97	120	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	90	104	–	86	100	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	–	100	400	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	+12.0	±12.6	–	±11.0	±12.6	–	V

NOTE 1: Exclude first hour of operation to allow for stabilization of external circuitry.
NOTE 2: This parameter is tested on a sample basis only, and guaranteed to an LTPD of 10.

SIMPLIFIED SCHEMATIC

MPOP05, MPOP07, MPOP10 (either side)



= R2A and R2B are electronically adjusted during factory test for minimum V_{OS} (MP5507 only).

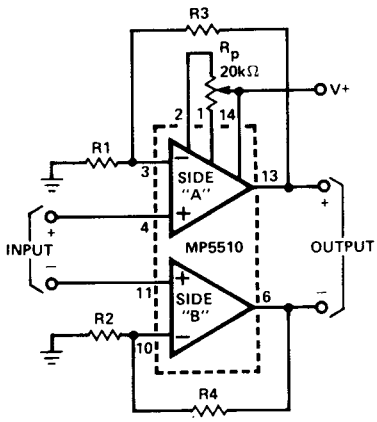


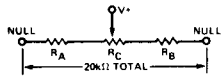
FIGURE 1

OFFSET TRIMMING MPOP10

Where voltage offset match between op-amps is critical, offset trimming of one or both sides of the MPOP10 may be necessary. Best drift performance will be obtained using a 20K potentiometer giving approximately ±4mV of V_{OS} adjustment. Although each amplifier is provided with its own set of offset trimming terminals, only one side needs to be trimmed. Trimming the V_{OS} of side A (or side B) to meet the V_{OS} of the other side will result in a V_{OS} difference of zero. (Figure 1.)

Similar results can be obtained by individually adjusting each side to zero offset. Performance over temperature is guaranteed using either method. In trimming applications requiring less V_{OS} adjustment but greater potentiometer resolution, the circuit in figure 2 should be used.

FIGURE 2



MODEL	NULL RANGE	FIXED RESISTORS R_A, R_B	POTENTIOMETER R_C
MP5510AY, MP5510BY, MP5510EY	±1.2mV	5.1kΩ	10.0kΩ

4

MATCHING PARAMETER DEFINITIONS, MPOP10

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS})
The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$). In figure at right, if $V_{OSA} = V_{OSB}$, the net differential offset voltage at the output of the amplifier pair is zero.

INPUT OFFSET VOLTAGE TRACKING ($TC\Delta V_{OS}$)
The ratio of the change in ΔV_{OS} to the change in temperature producing it.

AVERAGE NON-INVERTING BIAS CURRENT (I_{B^+})
The average of the side A and side B non-inverting input bias currents.

$$\frac{I_{BA^+} + I_{BB^+}}{2}$$

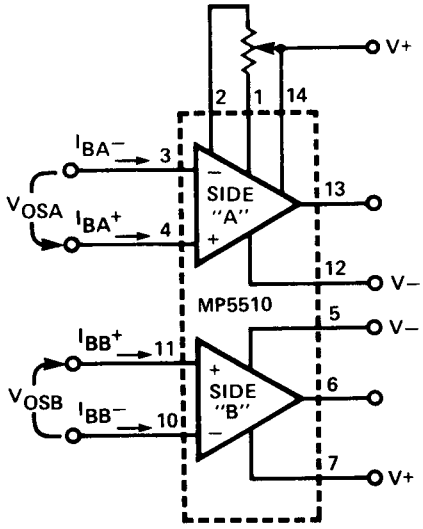
NON-INVERTING INPUT OFFSET CURRENT (I_{OS^+})
The difference between the non-inverting input bias currents of side A and side B; ($I_{BA^+} - I_{BB^+}$).

INVERTING INPUT OFFSET CURRENT (I_{OS^-})
The difference between the inverting input bias currents of side A and side B; ($I_{BA^-} - I_{BB^-}$).

AVERAGE DRIFT OF NON-INVERTING BIAS CURRENT (TCI_{B^+})
The ratio of the change in non-inverting bias current to the change in temperature producing it.

AVERAGE DRIFT OF NON-INVERTING OFFSET CURRENT (TCI_{OS^+}) The ratio of the change in non-inverting offset current to the change in temperature producing it.

COMMON MODE REJECTION RATIO MATCH ($\Delta CMRR$)
The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. $\Delta CMRR$ in dB = $20 \log_{10}$ ($\Delta CMRR$ in volt/volt).

SUPPLY VOLTAGE REJECTION RATIO MATCH ($\Delta PSRR$)
The difference between the power supply rejection ratios (expressed in volt/volt) of side A and side B. $\Delta PSRR$ in dB = $20 \log_{10}$ ($\Delta PSRR$ in volt/volt).

CHANNEL SEPARATION.
The ratio of the change in input offset voltage of one channel to the change in output voltage in the second channel producing it.