

# European Computer Controlled Teletext Circuit (EURO CCT)

# SAA5240

## GENERAL DESCRIPTION

The SAA5240 is a MOS N-channel integrated circuit which performs all the digital logic functions of a 625-line World System Teletext decoder. It operates in conjunction with the teletext video processor SAA5230, standard static RAM's and is controlled via the 2-wire I<sup>2</sup>C bus. The device can be used to provide videotex display conforming to a serial character attribute protocol.

### Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 6 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language selection of up to three different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Ghost row reception option (extension packets)
- Standard I<sup>2</sup>C bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets: SAA5240A; English, German, Swedish SAA5240B; Italian, German, French

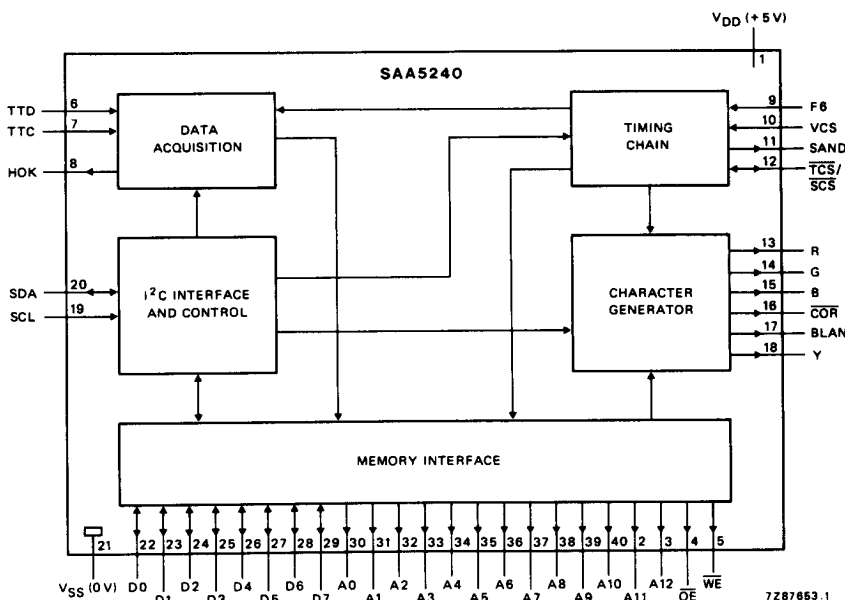


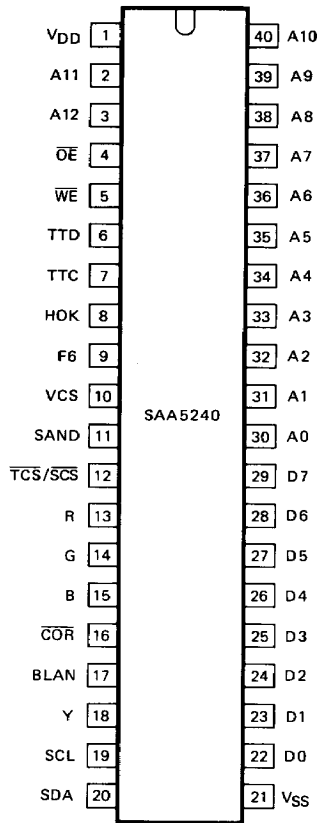
Fig. 1 Block diagram.

## PACKAGE OUTLINES

40-lead DIL; plastic (SOT-129).

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Fig. 2 Pinning diagram.

**PINNING**

- 1            VDD            **Power supply:** + 5 V power supply pin.
- 2, 3, 40    A11, A12, A10    **Chapter Address:** three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.
- 4            OE            **Output Enable:** active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.
- 5            WE            **Write Enable:** active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
- 6            TTD            **Teletext Data:** input from the SAA5230 Video Input Processor (VIP2). It is clamped to VSS for 4 to 8 μs of each television line to maintain the correct d.c. level following the external a.c. coupling.

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7	TTC	<b>Teletext Clock:</b> 6,9375 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
8	HOK	<b>Hamming O.K.:</b> an active high output signal indicating reception of a valid teletext data line with no Hamming errors in the magazine or row bytes. It is reset at line rate.
9	F6	<b>Character display clock:</b> 6 MHz clock input from the SAA5230. It is internally a.c. coupled to an active clamp input buffer.
10	VCS	<b>Video Composite Sync:</b> input from the SAA5230 derived from the incoming video signal. Sync pulses are active high.
11	SAND	<b>Sandcastle:</b> 3-level sandcastle output to the SAA5230 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS/SCS}}$	<b>Text Composite Sync/Scan Composite Sync:</b> as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig. 6) which is fed to the SAA5230 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	<b>Red, Blue, Green:</b> these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	<b>Contrast Reduction:</b> open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	<b>Blanking:</b> open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	<b>Character foreground:</b> open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	<b>Serial Clock:</b> input signal which is the I <sup>2</sup> C bus clock from the microcontroller.
20	SDA	<b>Serial Data:</b> is the I <sup>2</sup> C bus data line. It is an input/output function with an open drain output.
21	VSS	<b>Ground:</b> 0 volts.
22-29	DO-D7	<b>8 RAM data lines:</b> 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	<b>RAM address:</b> 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

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**European Computer Controlled Teletext Circuit (EURO CCT)**
**SAA5240****RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 1)	$V_{DD}$	-0,3 to +7,5 V
Input voltage range		
VCS, SDA, SCL, D0-D7	$V_I$	-0,3 to +7,5 V
TTC, TTD, F6, $\overline{TCS/SCS}$	$V_I$	-0,3 to +13,2 V
Output voltage range		
SAND, A0-A12, $\overline{OE}$ , $\overline{WE}$ , D0-D7, SDA, HOK	$V_O$	-0,3 to +7,5 V
R, G, B, BLAN, $\overline{COR}$ , Y, $\overline{TCS/SCS}$	$V_O$	-0,3 to +13,2 V
Storage temperature range	$T_{stg}$	-20 to +125 °C
Operating ambient temperature range	$T_{amb}$	-20 to +70 °C

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## CHARACTERISTICS

 $V_{DD} = 5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
<b>SUPPLY</b>					
Supply voltage (pin 1)	$V_{DD}$	4,5	5,0	5,5	V
Supply current (pin 1)	$I_{DD}$	—	160	—	mA
<b>INPUTS (note 1)</b>					
<b>TTD (note 2)</b>					
External coupling capacitor	$C_{ext}$	—	—	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2,0	—	7,0	V
Input data rise and fall times (note 3)	$t_r, t_f$	10	—	80	ns
Input data set-up time (note 4)	$t_{DS}$	40	—	—	ns
Input data hold time (note 4)	$t_{DH}$	40	—	—	ns
Input leakage current at $V_I = 0$ to $10\text{ V}$	$I_{LI}$	—	—	20	$\mu\text{A}$
Input capacitance	$C_I$	—	—	7	pF
<b>TTC; F6 (note 5)</b>					
D.C. input voltage range	$V_I$	-0,3	—	+ 10,0	V
A.C. input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,0	—	7,0	V
Input peaks relative to 50% duty cycle	$\pm V_p$	0,2	—	3,5	V
TTC clock frequency	$f_{TTC}$	—	6,9375	—	MHz
F6 clock frequency	$f_{F6}$	—	6,0	—	MHz
Clock rise and fall times (note 3)	$t_r, t_f$	10	—	80	ns
Input leakage current at $V_I = 0$ to $10\text{ V}$	$I_{LI}$	—	—	20	$\mu\text{A}$
Input capacitance	$C_I$	—	—	7	pF
<b>VCS</b>					
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input voltage HIGH	$V_{IH}$	2,0	—	$V_{DD}$	V
Input rise and fall times (note 3)	$t_r, t_f$	—	—	500	ns
Input leakage current at $V_I = 5,5\text{ V}$	$I_{LI}$	—	—	10	$\mu\text{A}$
Input capacitance	$C_I$	—	—	7	pF

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## CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>SCL</b>					
Input voltage LOW	$V_{IL}$	0	—	1,5	V
Input voltage HIGH	$V_{IH}$	3,0	—	$V_{DD}$	V
SCL clock frequency	$f_{SCL}$	0	—	100	kHz
Input rise and fall times (note 3)	$t_r, t_f$	—	—	2	$\mu s$
Input leakage current at $V_I = 5,5$ V	$I_{LI}$	—	—	10	$\mu A$
Input capacitance	$C_I$	—	—	7	pF
<b>INPUT/OUTPUTS (note 6)</b>					
<b><math>\overline{TCS}</math> (output)/<math>\overline{SCS}</math> (input)</b>					
Input voltage LOW	$V_{IL}$	0	—	1,5	V
Input voltage HIGH	$V_{IH}$	3,5	—	10,0	V
Input rise and fall times (note 3)	$t_r, t_f$	—	—	500	ns
Input leakage current at $V_I = 0$ to 10 V and output in high impedance state	$\pm I_{LI}$	—	—	10	$\mu A$
Input capacitance	$C_I$	—	—	7	pF
Output voltage LOW at $I_{OL} = 1,6$ mA	$V_{OL}$	0	—	0,4	V
Output voltage HIGH at $-I_{OH} = 0,2$ mA at $I_{OH} = 0,1$ mA	$V_{OH}$ $V_{OH}$	2,4 2,4	— —	$V_{DD}$ 6,0	V V
Output rise and fall times between 0,6 V and 2,2 V levels	$t_r, t_f$	—	—	100	ns
Load capacitance	$C_L$	—	—	50	pF
<b>SDA (note 7)</b>					
Input voltage LOW	$V_{IL}$	0	—	1,5	V
Input voltage HIGH	$V_{IH}$	3,0	—	$V_{DD}$	V
Input rise and fall times (note 3)	$t_r, t_f$	—	—	2	$\mu s$
Input leakage current at $V_I = 5,5$ V with output off	$I_{LI}$	—	—	10	$\mu A$
Input capacitance	$C_I$	—	—	7	pF
Output voltage LOW at $I_{OL} = 3$ mA	$V_{OL}$	0	—	0,5	V
Output fall time between 3,0 V and 1,0 V levels	$t_f$	—	—	200	ns
Load capacitance	$C_L$	—	—	400	pF

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parameter	symbol	min.	typ.	max.	unit
<b>INPUT/OUTPUTS (continued)</b>					
<b>D0-D7 (note 8)</b>					
Input voltage LOW	$V_{IL}$	0	—	0,8	V
Input voltage HIGH	$V_{IH}$	2,0	—	$V_{DD}$	V
Input leakage current at $V_I = 0\text{ V}$ to 5,5 V and output in high impedance state	$\pm I_{LI}$	—	—	10	$\mu\text{A}$
Input capacitance	$C_I$	—	—	7	pF
Output voltage LOW at $I_{OL} = 1,6\text{ mA}$	$V_{OL}$	0	—	0,4	V
Output voltage HIGH at $-I_{OH} = 0,2\text{ mA}$	$V_{OH}$	2,4	—	$V_{DD}$	V
Output rise and fall times between 0,6 V and 2,2 V levels	$t_r, t_f$	—	—	50	ns
Load capacitance	$C_L$	—	—	120	pF
<b>OUTPUTS (note 6)</b>					
<b>A0-A12; <math>\overline{OE}</math>; <math>\overline{WE}</math> (note 8)</b>					
Output voltage LOW at $I_{OL} = 1,6\text{ mA}$	$V_{OL}$	0	—	0,4	V
Output voltage HIGH at $-I_{OH} = 0,2\text{ mA}$	$V_{OH}$	2,4	—	$V_{DD}$	V
Output rise and fall times between 0,6 V and 2,2 V levels	$t_r, t_f$	—	—	50	ns
Load capacitance	$C_L$	—	—	120	pF
<b>H0K (note 9)</b>					
Output voltage LOW at $I_{OL} = 1,6\text{ mA}$	$V_{OL}$	0	—	0,4	V
Output voltage HIGH at $-I_{OH} = 0,2\text{ mA}$	$V_{OH}$	2,4	—	$V_{DD}$	V
Output rise and fall times between 0,6 V and 2,2 V levels	$t_r, t_f$	—	—	100	ns
Load capacitance	$C_L$	—	—	50	pF
<b>SAND (note 9)</b>					
Output voltage LOW at $I_{OL} = 0,2\text{ mA}$	$V_{OL}$	0	—	0,2	V
Output voltage INTERMEDIATE at $I_{OL} = \pm 30\ \mu\text{A}$	$V_{OI}$	1,3	—	2,7	V

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## CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
<b>SAND (continued)</b>					
Output voltage HIGH at $I_{OH} = 0$ to $-30 \mu A$	$V_{OH}$	4,2	—	$V_{DD}$	V
Output rise time $V_{OL}$ to $V_{OI}$ between 0,4 V and 1,1 V levels	$t_{r1}$	—	—	400	ns
Output rise time $V_{OI}$ to $V_{OH}$ between 2,9 V and 4,0 V levels	$t_{r2}$	—	—	200	ns
Output fall time $V_{OH}$ to $V_{OL}$ between 4,0 V and 0,4 V levels	$t_f$	—	—	50	ns
Load capacitance	$C_L$	—	—	30	pF
<b>R; G; B; <math>\overline{COR}</math>; BLAN; Y (note 10)</b>					
Output voltage LOW at $I_{OL} = 2$ mA	$V_{OL}$	0	—	0,4	V
Output voltage LOW at $I_{OL} = 5$ mA	$V_{OL}$	0	—	1,0	V
Pull-up voltage as seen at pin	$V_{PU}$	—	—	6,0	V
Output fall time with a load resistor of $1,2$ k $\Omega$ to 6 V and measured between 5,5 V and 1,5 V	$t_f$	—	—	20	ns
Skew delay between outputs with a load resistor of $1,2$ k $\Omega$ to 6 V and measured on the falling edges at 3,5 V	$t_{SK}$	—	—	20	ns
Load capacitance	$C_L$	—	—	25	pF
Output leakage current at $V_{PU} = 0$ to 6 V with output off	$I_{LO}$	—	—	10	$\mu A$
<b>TIMING</b>					
<b>I<sup>2</sup>C bus (note 11)</b>					
Clock low period	$t_{LOW}$	4	—	—	$\mu s$
Clock high period	$t_{HIGH}$	4	—	—	$\mu s$
Data set-up time	$t_{SU}; DAT$	250	—	—	ns
Data hold time	$t_{HD}; DAT$	0	—	—	ns
Stop set-up time from clock high	$t_{SU}; STO$	4	—	—	$\mu s$
Start set-up time following a stop	$t_{BUF}$	4	—	—	$\mu s$
Start hold time	$t_{HD}; STA$	4	—	—	$\mu s$
Start set-up time following clock low to high transition	$t_{SU}; STA$	4	—	—	$\mu s$

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parameter	symbol	min.	typ.	max.	unit
<b>TIMING (continued)</b>					
<b>Memory interface (note 12)</b>					
Cycle time	t <sub>CY</sub>	—	500	—	ns
Address change to $\overline{OE}$ LOW	t <sub>OE</sub>	60	—	—	ns
Address active time	t <sub>ADDR</sub>	450	500	—	ns
$\overline{OE}$ pulse duration	t <sub>OEW</sub>	320	—	—	ns
Access time from $\overline{OE}$ to data valid	t <sub>ACC</sub>	—	—	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t <sub>DH</sub>	0	—	—	ns
Address change to $\overline{WE}$ LOW	t <sub>WE</sub>	40	—	—	ns
$\overline{WE}$ pulse duration	t <sub>WEW</sub>	200	—	—	ns
Data set-up time to $\overline{WE}$ HIGH	t <sub>DS</sub>	100	—	—	ns
Data hold time from $\overline{WE}$ HIGH	t <sub>DHWE</sub>	20	—	—	ns
Write recovery time	t <sub>WR</sub>	25	—	—	ns

**Notes to the characteristics**

- All inputs are protected against static charge under normal handling.
- The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig. 3).
- Rise and fall times between 10% and 90% levels.
- Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1  $\geq$  2,0 V; data stable 0  $\leq$  0,8 V (see Fig. 4).
- The TTC and F6 inputs have internal clamping diodes and are a.c. coupled (see Fig. 3).
- All outputs and input/outputs are protected against static charge under normal handling and connection to V<sub>DD</sub> and V<sub>SS</sub>.
- For details of I<sup>2</sup>C bus timing see Fig. 8.
- For details of RAM timing see Fig. 9.
- For details of synchronization and HOK timing see Fig. 5.
- For details of display output timing see Fig. 7.
- The I<sup>2</sup>C bus timings are referred to V<sub>IH</sub> = 3 V and V<sub>IL</sub> = 1,5 V. For waveforms see Fig. 8.
- The memory interface timings are referred to V<sub>IL</sub> = 1,5 V. For waveforms see Fig. 9.

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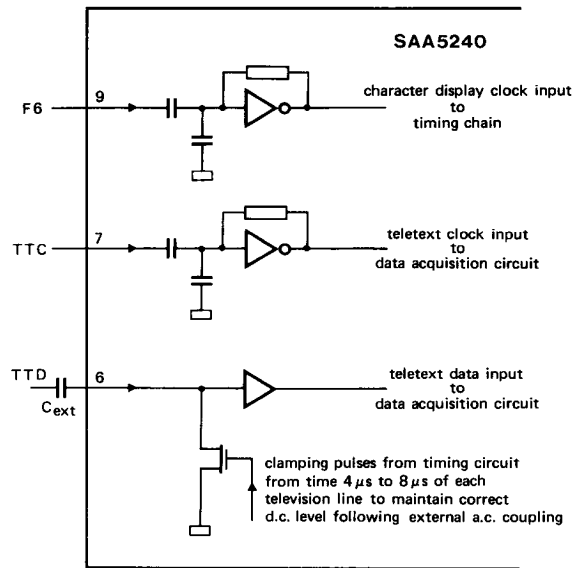
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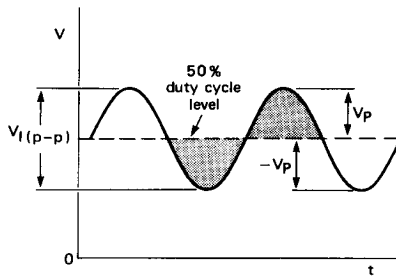
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(a)



shaded regions equal in area

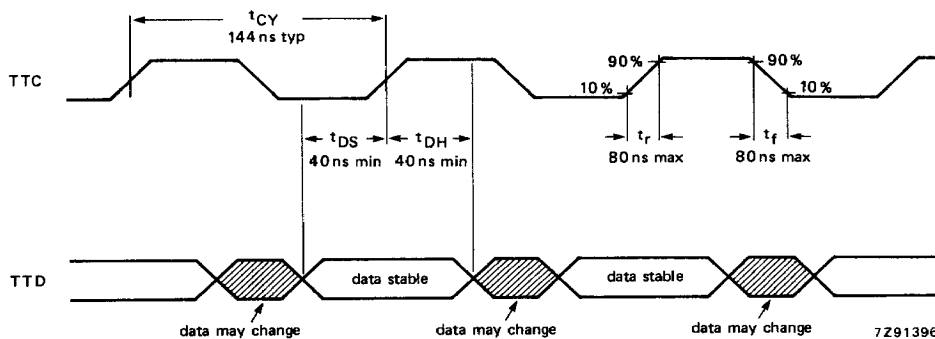
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(b)

Fig. 3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.

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Data stable: 1 is  $\geq 2,0 \text{ V}$ ; 0 is  $\leq 0,8 \text{ V}$ .

Fig. 4 Teletext data input timing.

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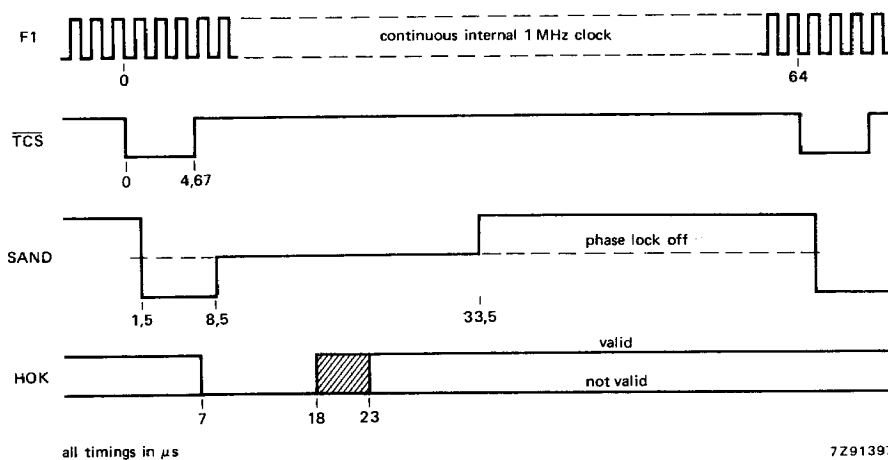
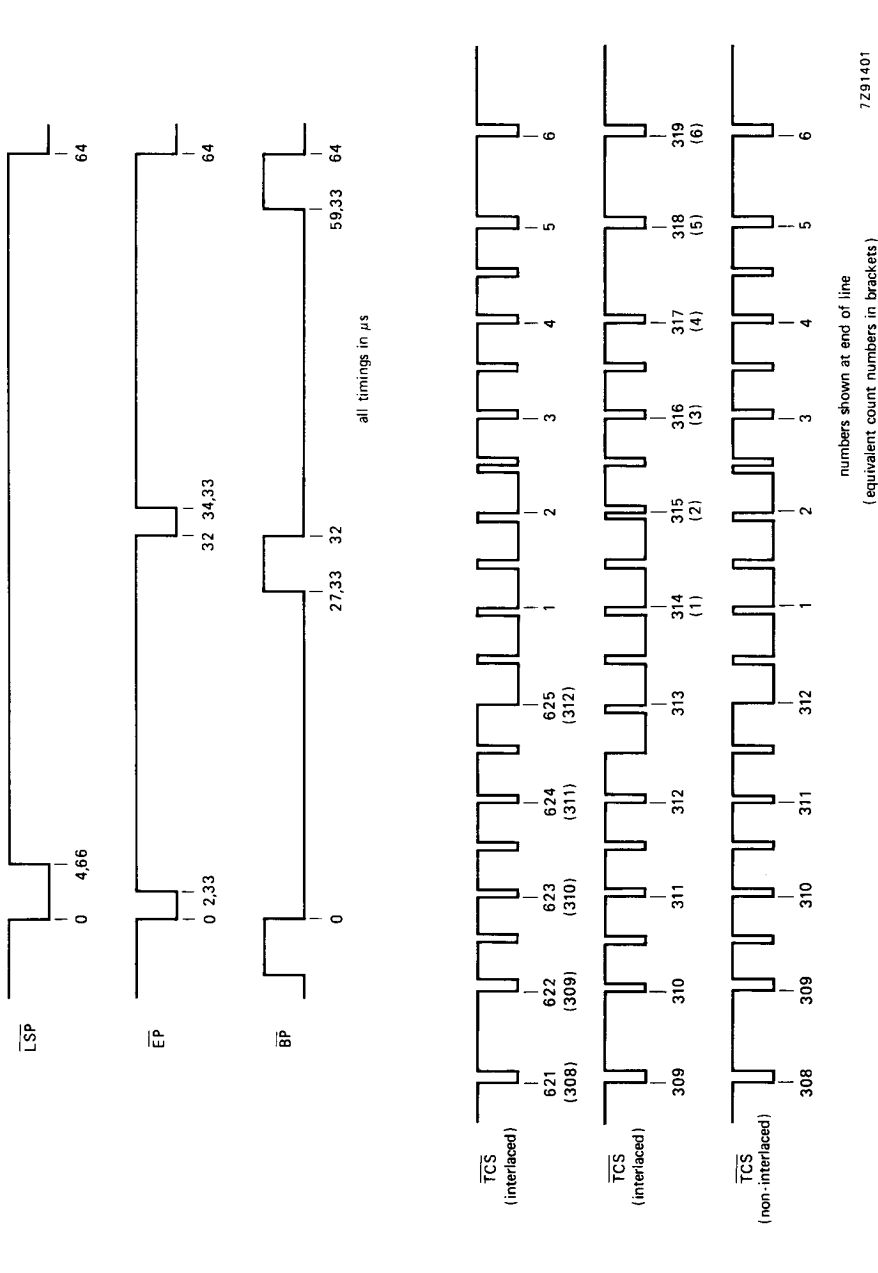


Fig. 5 Synchronization and HOK timing.

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Line sync pulses ( $\overline{LSP}$ ), equalizing pulses ( $\overline{EP}$ ) and broad pulses ( $\overline{BP}$ ) are combined to provide the text composite sync waveform ( $\overline{TCS}$ ) as shown.

All timings measured from falling edge of  $\overline{LSP}$  with a tolerance of  $\pm 100$  ns.

Fig. 6 Composite sync waveforms.

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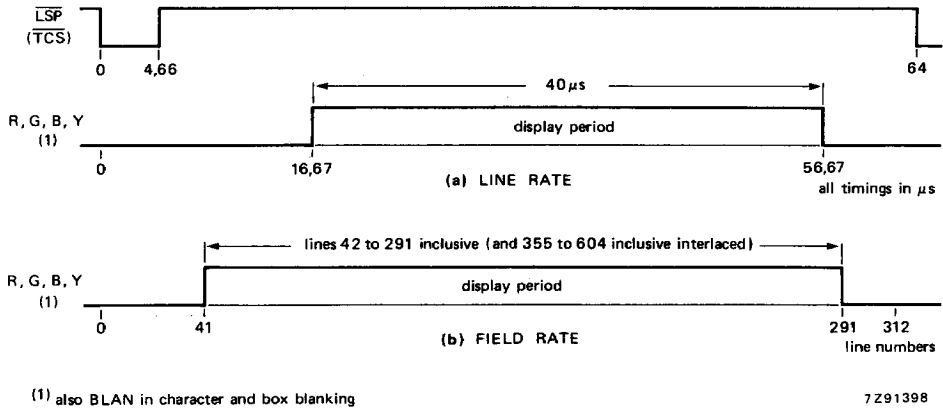


Fig. 7 Display output timing (a) line rate (b) field rate.

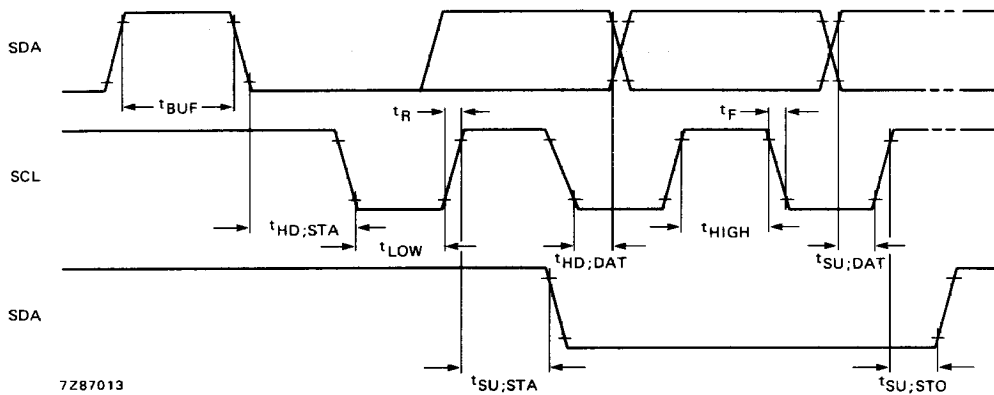
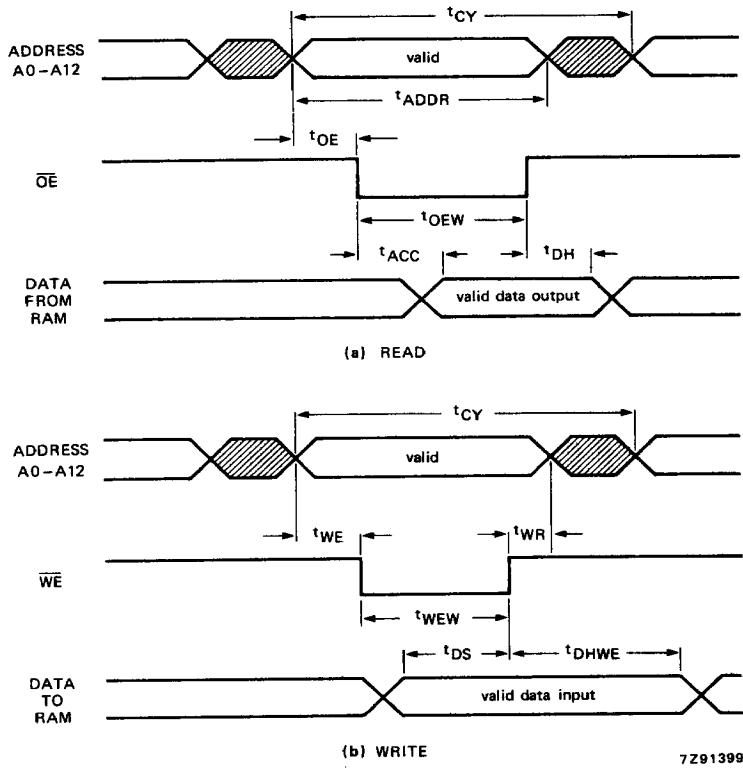


Fig. 8 I<sup>2</sup>C bus timing.

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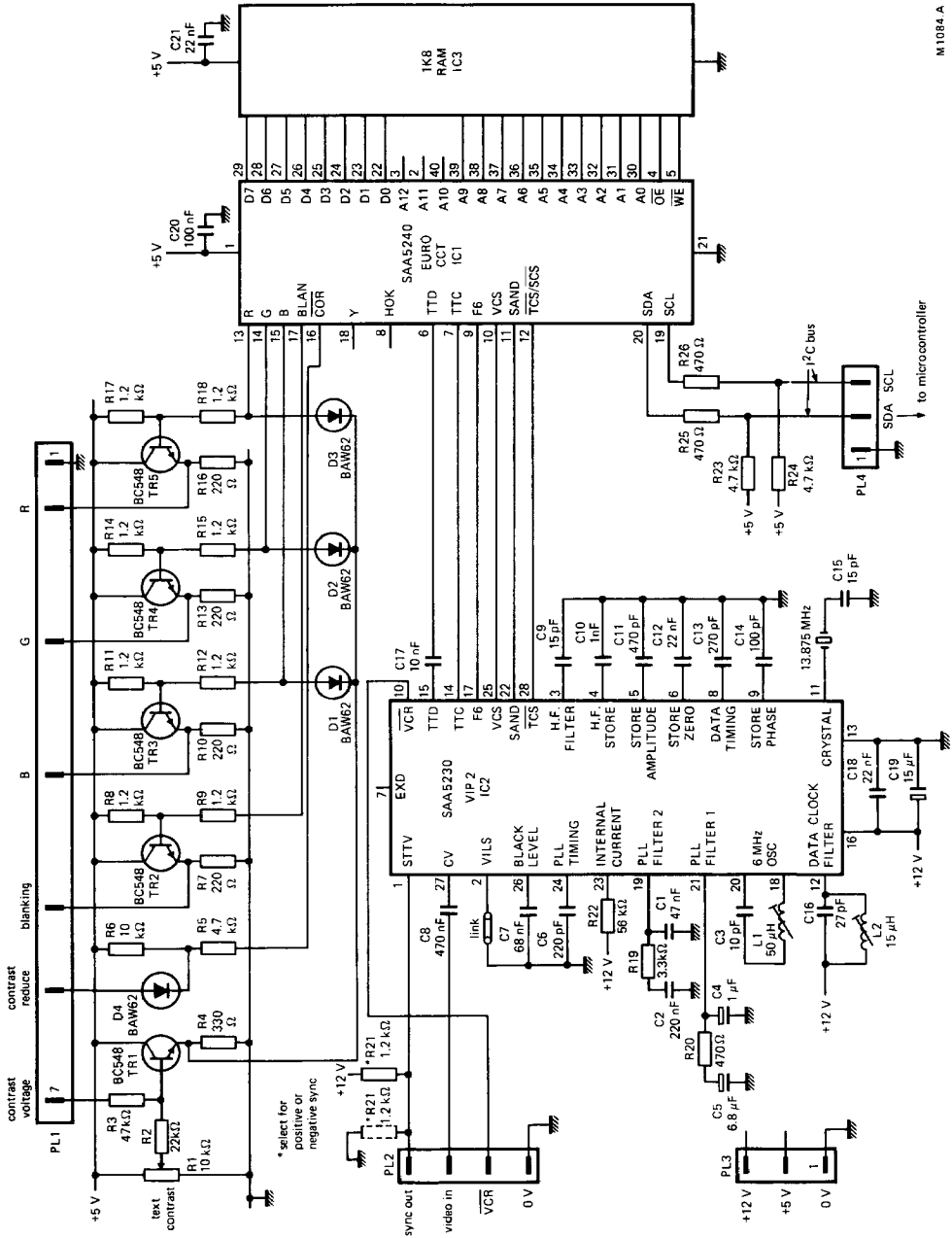
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Fig. 9 Memory interface timing (a) read (b) write.

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## APPLICATION INFORMATION



M1084.A

Fig. 10 EURO CCT based single-page decoder circuit diagram.



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## APPLICATION INFORMATION (continued)

### EURO CCT page memory organization

The organization of a page memory is shown in Fig. 11. The EURO CCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF CCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

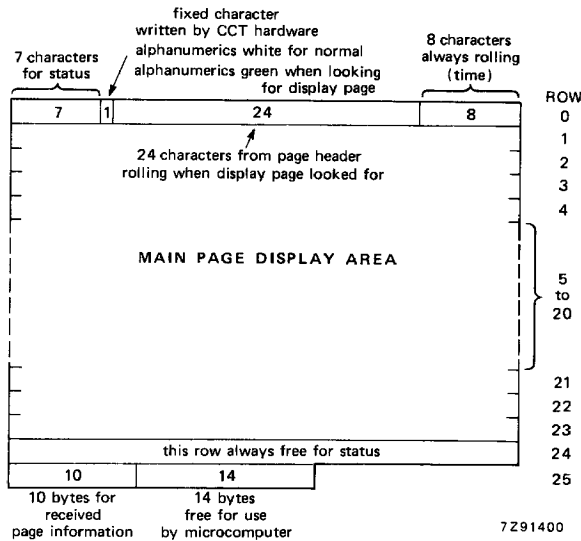


Fig. 11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	FOUND	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0

Column 0 1 2 3 4 5 6 7 8 9

Where:

- |        |                                     |               |            |                          |                 |
|--------|-------------------------------------|---------------|------------|--------------------------|-----------------|
| MAG    | magazine                            | } page number | MU         | minutes units            | } page sub-code |
| PU     | page units                          |               | MT         | minutes tens             |                 |
| PT     | page tens                           |               | HU         | hours units              |                 |
| PBLF   | page being looked for               | HT            | hours tens |                          |                 |
| FOUND  | LOW for page has been found         |               | C4-C14     | transmitted control bits |                 |
| HAM.ER | Hamming error in corresponding byte |               |            |                          |                 |

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*Row 0*

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by EURO CCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

*Row 25*

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

**Register maps**

EURO CCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.

Register map (R3), for page requests, is shown in detail in Table 3.

**Table 2** EURO CCT register map

D7	D6	D5	D4	D3	D2	D1	D0	
TA	$\overline{7+P}$ / 8 BIT	ACQ. ON/OFF	GHOST ROW ENABLE	$\overline{DEW}$ / FULL FIELD	TCS ON	T1	T0	R1 Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2 Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3 Page request data
—	—	—	—	—	A2	A1	A0	R4 Display chapter
BKGN OUT	BKGN IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5 Display control (normal)
BKGN OUT	BKGN IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6 Display control (newsflash/subtitle)
STATUS ROW BTM/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$ / REVEAL	$\overline{\text{TOP}}$ / BOTTOM	SINGLE/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7 Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8 Active chapter
—	—	—	R4	R3	R2	R1	R0	R9 Active row
—	—	C5	C4	C3	C2	C1	C0	R10 Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11 Active data

— bit does not exist

**Notes to Table 2**

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I<sup>2</sup>C transmission byte. TA and TB must be logic 0 for normal operation.

All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.

All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

## European Computer Controlled Teletext Circuit (EURO CCT)

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**APPLICATION INFORMATION** (continued)**Table 2** (continued)

Where:

R1 Mode

T0, T1

TCS ON

DEW/FULL FIELD

7 + P/8 BIT

TA, TB

R2 Page request address

START COLUMN

ACQ CCT

BANK SELECT

R3 Page request data

R4 Display chapter

R5, R6 Display control

PON

TEXT

COR

BKGND

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 Display mode

BOX ON 0 (1-23, 24)

STATUS ROW BTM/TOP

R8 to R11

interlace/non interlace 312/313 line control

text composite sync or direct sync select

field-flyback or full channel mode

7 bits with parity checking or 8-bit mode

test bits; 0 for normal operation

start column for page request data

selects one of four acquisition circuits

selects bank of four pages being addressed for acquisition

see Table 3

determines which of the 8 pages is displayed

for normal and newflash/subtitle

picture on

text on

contrast reduction on

background colour on

boxing function allowed on row 0 (row 1-23, 24)

row 25 displayed above or below the main text

active chapter, row, column and data information written to or read from page memory via the I<sup>2</sup>C bus.

## European Computer Controlled Teletext Circuit (EURO CCT)

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**Table 3** Register map for page requests (R3)

Start Column	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

**Notes to Table 3**

Abbreviations are as for Table 1 except for D0 CARE bits.

When the D0 CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the D0 CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.

If  $\overline{\text{HOLD}}$  is set LOW, the page is held and not updated.

There are four groups of data shown in Table 3, one for each acquisition circuit (four simultaneous page requests).

Columns auto-increment on successive I<sup>2</sup>C transmission bytes.

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# European Computer Controlled Teletext Circuit (EURO CCT)

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## APPLICATION INFORMATION (continued)

### CHARACTER SETS

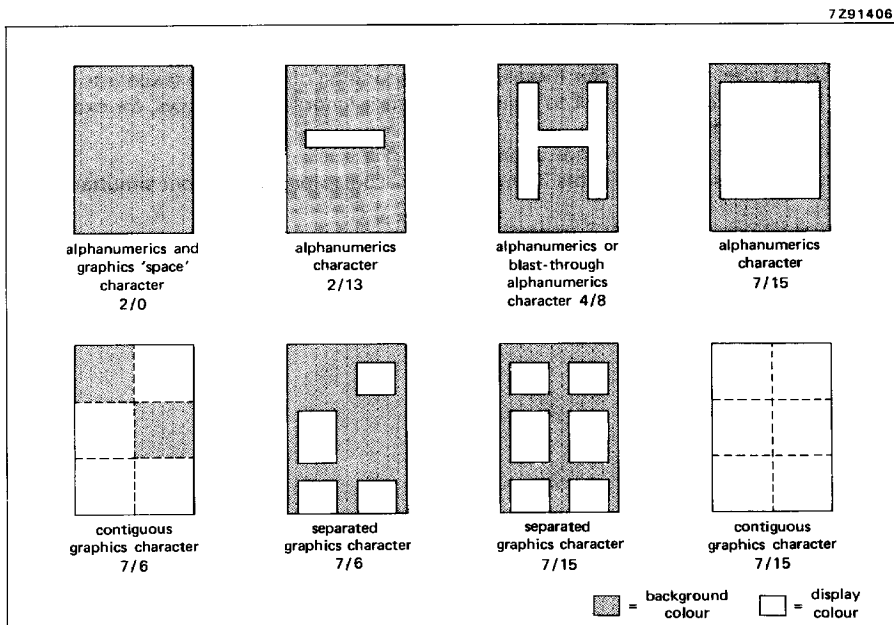
The UK teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14 as shown in Table 4. The basic 96 character sets differ only in the 13 national option characters as indicated in Tables 8 and 9 with reference to their table position in the basic character matrix shown in Table 7. EURO CCT automatically decodes control bits C12 to C14. Other combinations of C12 to C14 are defaulted to SAA5240A (English); SAA5240B (German). With 8-bit decoding the character matrices are shown in Tables 5 and 6.

**Table 4** Selection of national character sets

PHCB	ENGLISH	GERMAN	SWEDISH	ITALIAN	FRENCH
C12	0	0	0	0	1
C13	0	0	1	1	0
C14	0	1	0	1	0

Where:

PHCB                      page header control bits.



**Fig. 12** Character format.

European Computer Controlled Teletext Circuit (EURO CCT)

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Table 5 Character data input decoding (SAA5240A)

BITS	column				0 or 1		0 or 1		0 or 1		0 or 1		1		1			
	b <sub>8</sub>	b <sub>7</sub>	b <sub>6</sub>	b <sub>5</sub>	0	1	0	1	0	1	0	1	0	1	0	1		
row	b <sub>4</sub>	b <sub>3</sub>	b <sub>2</sub>	b <sub>1</sub>	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9
0 0 0 0	0	0	0	0	alpha- numerics black	graphics black												
0 0 0 1	1	0	0	0	alpha- numerics red	graphics red												
0 0 1 0	0	0	1	0	alpha- numerics green	graphics green												
0 0 1 1	1	0	0	1	alpha- numerics yellow	graphics yellow												
0 1 0 0	0	1	0	0	alpha- numerics blue	graphics blue												
0 1 0 1	1	0	0	1	alpha- numerics magenta	graphics magenta												
0 1 1 0	0	1	0	1	alpha- numerics cyan	graphics cyan												
0 1 1 1	1	0	1	1	alpha- numerics white	graphics white												
1 0 0 0	0	0	0	0	flash	conceal display												
1 0 0 1	1	0	0	1	steady	contiguous graphics												
1 0 1 0	0	1	0	0	end box	separated graphics												
1 0 1 1	1	0	1	1	start box	ESC												
1 1 0 0	0	1	0	0	normal height	black back- ground												
1 1 0 1	1	1	0	1	double height	new back- ground												
1 1 1 0	0	1	1	0	SO	hold graphics												
1 1 1 1	1	1	1	1	SI	release graphics												

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\* These control characters are reserved for compatibility with other data codes.

\*\* These control characters are presumed before each row begins.

European Computer Controlled Teletext Circuit (EURO CCT)

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APPLICATION INFORMATION (continued)

Table 6 Character data input decoding (SAA5240B)

B T S	b <sub>8</sub> →				b <sub>7</sub> →		b <sub>6</sub> →		b <sub>5</sub> →		0 or 1		0 or 1		0 or 1		0 or 1		1		1	
	0	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub>	column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9							
row	0	1	2	3	4	5	6	7	8	9												
0 0 0 0	alpha- numerics black	graphics black			0			é	P	ü		p		š	à							
0 0 0 1	alpha- numerics red	graphics red	!		1			A	Q	a		q		°	é							
0 0 1 0	alpha- numerics green	graphics green	"		2			B	R	b		r		ä	ä							
0 0 1 1	alpha- numerics yellow	graphics yellow	£		3			C	S	c		s		#	é							
0 1 0 0	alpha- numerics blue	graphics blue	\$		4			D	T	d		t		\$	i							
0 1 0 1	alpha- numerics magenta	graphics magenta	%		5			E	U	e		u		€	€							
0 1 1 0	alpha- numerics cyan	graphics cyan	&		6			F	V	f		v		©	©							
0 1 1 1	alpha- numerics white**	graphics white**	'		7			G	W	g		w		?	?							
1 0 0 0	flash	conceal display	(		8			H	X	h		x		ö	ö							
1 0 0 1	steady**	contiguous graphics**	)		9			I	Y	i		y		ü	ü							
1 0 1 0	end box**	separated graphics**	*		:			J	Z	j		z		ß	ç							
1 0 1 1	start box	ESC*	+		:			K	°	k		à		ř	ë							
1 1 0 0	normal height**	black back- ground**	,		^			L	ç	l		ó		ö	ë							
1 1 0 1	double height	new back- ground	-		=			M	→	m		é		ü	ü							
1 1 1 0	SO*	hold graphics	.		Y			N	↑	n		i		^	I							
1 1 1 1	SI*	release graphics**	/		?			O	#	o					#							

\* These control characters are reserved for compatibility with other data codes.

\*\* These control characters are presumed before each row begins.

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**European Computer Controlled Teletext Circuit (EURO CCT)**

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**SAA5240****Notes to Tables 5 and 6**

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows:
5. The SAA5240A national option characters are shown in Table 8.
6. The SAA5240B national option characters are shown in Table 9.
7. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters to combine with character 8/5.
8. With bit 8 = 0 national option characters will be decoded according to the setting of control bits C12 to C14 (see Table 4).

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European Computer Controlled Teletext Circuit (EURO CCT)

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APPLICATION INFORMATION (continued)  
Table 7 SAA5240 basic character matrix

2/0		2/8		3/0		3/8		4/0	NC	4/8		5/0		5/8		6/0	NC	6/8		7/0		7/8	
2/1		2/9		3/1		3/9		4/1		4/9		5/1		5/9		6/1		6/9		7/1		7/9	
2/2		2/10		3/2		3/10		4/2		4/10		5/2		5/10		6/2		6/10		7/2		7/10	
2/3	NC	2/11		3/3		3/11		4/3		4/11		5/3		5/11	NC	6/3		6/11		7/3		7/11	NC
2/4	NC	2/12		3/4		3/12		4/4		4/12		5/4		5/12	NC	6/4		6/12		7/4		7/12	NC
2/5		2/13		3/5		3/13		4/5		4/13		5/5		5/13	NC	6/5		6/13		7/5		7/13	NC
2/6		2/14		3/6		3/14		4/6		4/14		5/6		5/14	NC	6/6		6/14		7/6		7/14	NC
2/7		2/15		3/7		3/15		4/7		4/15		5/7		5/15	NC	6/7		6/15		7/7		7/15	

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Where: NC national option character position.

European Computer Controlled Teletext Circuit (EURO CCT)

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Table 8 SAA5240A character set (national option characters)

ENGLISH

2/3	2/4	4/0	5/11	5/12	5/13	5/14
5/15	6/0	7/11	7/12	7/13	7/14	

GERMAN

2/3	2/4	4/0	5/11	5/12	5/13	5/14
5/15	6/0	7/11	7/12	7/13	7/14	

SWEDISH

2/3	2/4	4/0	5/11	5/12	5/13	5/14
5/15	6/0	7/11	7/12	7/13	7/14	

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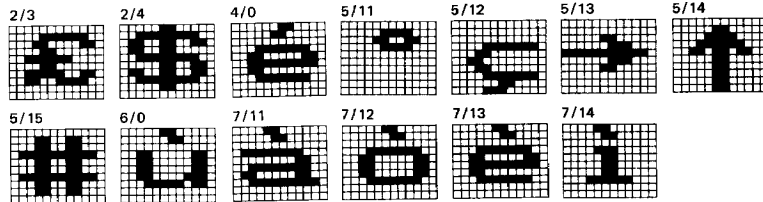
European Computer Controlled Teletext Circuit (EURO CCT)

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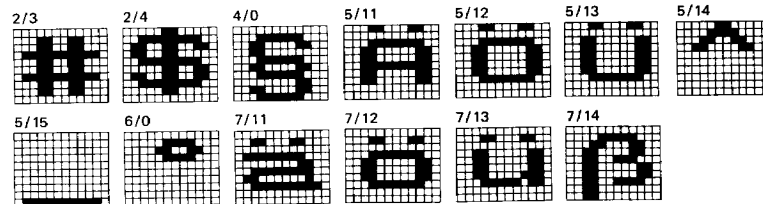
APPLICATION INFORMATION (continued)

Table 9 SAA5240B character set (national option characters)

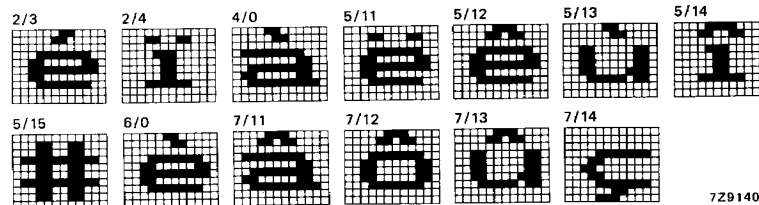
ITALIAN



GERMAN



FRENCH



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Purchase of Philips' I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C-system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips.

For additional information  
consult the Applications Section.